REMARKS

Reconsideration of the above-identified application is requested in view of the remarks that follow.

In the December 30, 2005, Office Action in this application, the Examiner objected to claims 1-6 because they included the following informality: "the wording 'the second portion' (line 15 of claim 1) should be replaced by 'a second portion."

As indicated above, claims 1-6 have been cancelled.

The Examiner rejected claims 1-3 and 5-8 under 35 U.S.C. §103(a) as being unpatentable over the Yama '657 reference in view of Applicant's Prior Art in the specification. Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over the Yama reference and Applicants' Prior Art and further in view of the Wolf reference.

As indicated above, claims 1-8 have been canceled. New claims 9-16 have been added. For the reasons set forth below, Applicant submits that new claims 9-16 patentably distinguish over the reference combination previously cited by the Examiner.

As stated in Applicants' specification, the present invention is directed to an ultra low leakage MOSFET transistor that is formed to minimize band-to-band and trap-assisted tunneling mechanisms that exist in prior art devices and can lead to gate induced drain leakage in the MOSFET transistor. In accordance with the invention, this design improvement is obtained by providing a new conductive gate electrode structure.

As show in Fig. 3 of the application, the conductive gate electrode of the claimed MOSFET transistor includes a first portion that extends over the substrate channel region and a second portion that extends continuously over the entire substantially rectangular interface between the isolation dielectric material and the active device region that the isolation dielectric material defines.

The Examiner relies on the Yama '657 patent to provide this teaching. However, Applicant submits that the Examiner must follow a tortured path to arrive at structural similarities between the Fig. 1A- 1C transistor structure disclosed by Yama and that shown in

Fig. 3 of the application. Specifically, Yama discloses a MOSFET transistor structure in which the drain includes a multiplicity of drain diffusion regions formed in the substrate and the source also includes a multiplicity of source diffusion regions formed in the same active device substrate. The gate electrode is a one solid piece of conductive material that extends over the entire active device region, except for open portions that expose the multiple drain regions and the multiple source regions so that a conductive interconnect structure be dropped down through vias in the dielectric material to contact the multiple drain regions and the multiple source regions. This is completely unlike the Applicant's Fig. 3 structure.

The Examiner selects one of the multiple drain diffusion regions of the Yama structure and one adjacent source diffusion region and utilizes this very small and limited aspect of the disclosed Yama MOSFET device structure and applied it to Applicants' claims. Again, the Yama structure relied upon by the Examiner has virtually no structural similarity to the source/drain and unique gate electrode structure shown in Applicant's Fig. 3 and recited in Applicant's new claims.

While Applicant submits that the Yama reference is misapplied to Applicant's claims, Applicant has cancelled the claims 1-8 and added new claims 9-16.

New independent claim 9 is directed essentially to the same structure recited in previously presented claim 1. The significant difference between new claim 9 and the MOSFET structure recited in previously presented, now canceled, claim 1 is that claim 9 recites a conductive gate electrode that "consists of" a first portion that extends over the substrate channel region and a second portion that extends continuously over the entire substantially rectangular interface between the isolation dielectric material and the active device region.

Similarly, new independent method claim 15 differs from previously presented method claim 6, now canceled, in that new method claim 15 recites a step of forming a conductive gate on the gate dielectric material, the conductive gate "consisting of" a first portion that extends over the substrate channel region and second portion that extends continuously over the entire interface between the isolation dielectric material and the active region.

Thus, both new claim 9 and new claim 15 recite a gate electrode structure that is neither taught nor suggested by the Yama reference. Applicant submits that there is nothing in the Yama reference, or the Wolf reference also cited by the Examiner, that hints of any appreciation of providing a MOSFET transistor structure that minimizes band-to-band and trap-assisted

tunneling mechanism that can lead to gate induced drain leakage characteristics. Therefore, Applicants submit that there is no motivation in any of the references cited by the Examiner, considered individually or in combination, to modify the teachings of any of the references to arrive at Applicants' invention as recited in new claims 9-16.

In view of the above, Applicant submits that all claims now present in this application patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

STALLMAN & POLLOCK LLP

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By: _____

Michael J. Pollock
Reg. No. 29,098

Attorneys for Applicant(s)